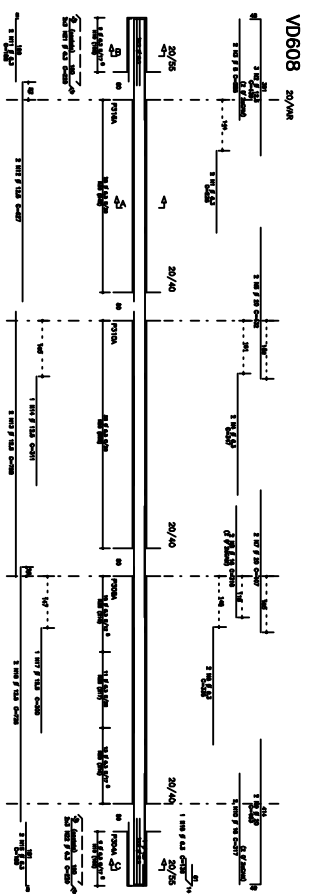
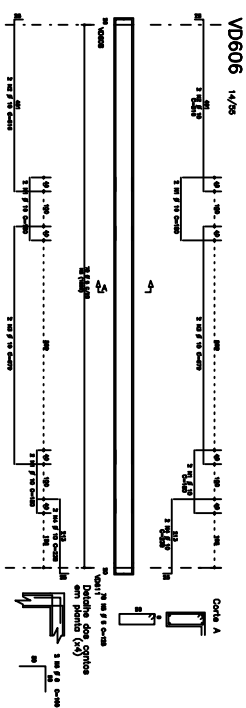
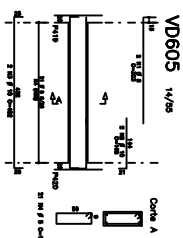
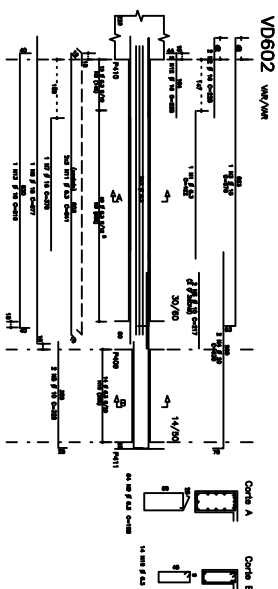
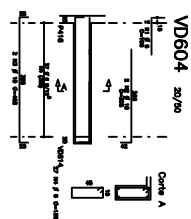
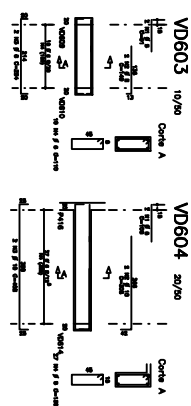
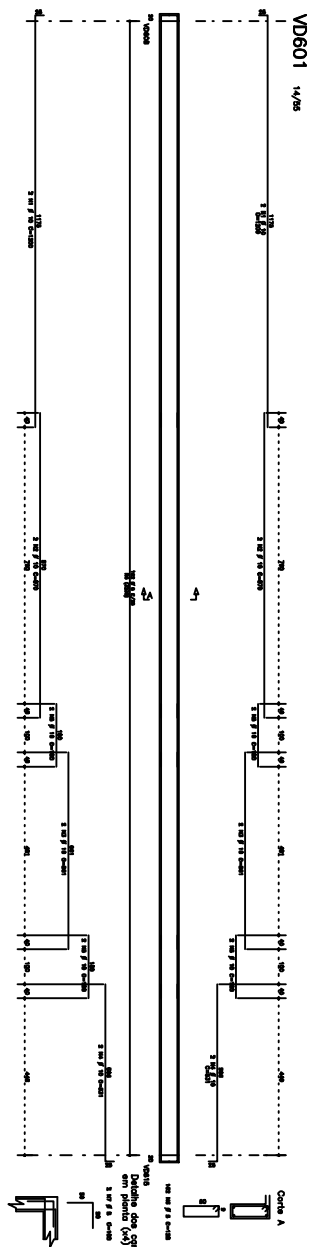


Figure 1: A detailed schematic diagram of a 16-bit parallel adder. The circuit consists of 16 input lines (A0-A15) and 16 output lines (S0-S15). The inputs are connected to a series of 1-bit full adders. The carry-in (Cin) is connected to the carry input of the first adder. The carry-out (Cout) of the final adder is connected back to the carry input of the first adder, forming a feedback loop. The sum outputs (S0-S15) are connected to the sum outputs of the adders. The diagram is labeled 'Figure 1' and '16-bit parallel adder'.

INDICE:
VD601 A VD606 / VD608 / VD609 / VD E60

FCK = 40 MPa
EC = 35 GPa
A/C = 0,65

$$A/C = 0,65$$
$$A/C = 0,65$$
[illegible]